Application Note 312
CMOS SOI RF Attenuator Family

Industry: Communications
Primary Applications: Wireless Communications

HIGH PERFORMANCE ATTENUATOR
INTRODUCTION
Honeywell has developed a line of highly integrated, low cost RF CMOS SOI (Silicon-On-Insulator) attenuators with integrated digital, mixed signal and RF functions. CMOS SOI technology provides the performance of GaAs with the economy and integration capabilities of conventional bulk CMOS. These attenuators are ideal for use in a wide range of wireless applications that require accuracy, speed and low power consumption. These devices were developed for use in cellular, PCS (Personal Communications Service) and GSM (Global System for Communications) base stations, handsets and 2.4 GHz WLAN (Wireless Local Area Network) applications.

CMOS SOI attenuators are manufactured using a high yield silicon process for superior integration of RF, passive and digital functions. Each chip incorporates active MOSFET transistor devices for RF, digital and mixed signal functions.

CMOS SOI ATTENUATOR FEATURES
• Integrated logic and drivers
• Very low DC power consumption
• Attenuation range of 0 dB to 31.5 dB
• Attenuation in steps of 0.5 dB or 1.0 dB
• Space saving QFN surface mount packaging
• Single supply operation
• Dual power supply configuration for improved linear RF power handling capability
• Parallel or serial digital interface
• 50 Ohm matched impedance
• High attenuation accuracy

BENEFITS
• Simplified digital interface
• Compact size
• Manufacturing cost savings
• Mature technology
• Volume production base

FUNCTIONAL SCHEMATIC

DEScriptions
RF Path The active RF path is composed of active microwave switch FETs that select the appropriate passive networks to the programmed attenuator value. The network is designed to maintain the 50 ohm input and output load regardless of attenuation settings to provide the best input and output return match.

Parallel Digital Interface The parallel digital interface pins are buffered, ESD protected and level-shifted prior to presentation to the RF attenuator circuits. Buffering guarantees that the required voltage levels are presented to the RF section as long as logic levels are valid at the chip inputs. Based on the level applied to VSS (see dual supply operation), signals may be level shifted to increase the P1dB compression point. Attenuation follows the truth table provided on the product data sheet.
**Serial Digital Interface** The digital interface circuits use a simple clock and data shift register. Data in the shift register is isolated from the data latches during the shift operation. After the proper data has been shifted in the register, a rising edge on the OE line will load the value in the register into the latches where it is held, defining the attenuation value, until the next load. All bits of the latch are loaded simultaneously.

**P1dB Level shifters** This device has an optional configuration to widen the linear range for higher power levels. With the VSS pin wired to default ground, this product has a P1dB in the low 20's dBm (refer to electrical specifications). With the VSS wired to a negative supply (up to -5 volts) proportionally 7 dB - 10 dB additional RF power can be applied prior to the P1dB compression point.

**ATTENUATOR FAMILY PRODUCTS**

<table>
<thead>
<tr>
<th>Listing</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HRF-AT4510</td>
<td>15.5 dB, DC-4 GHz, 5 Bit Parallel Digital Attenuator</td>
</tr>
<tr>
<td>HRF-AT4511</td>
<td>15.5 dB, DC-4 GHz, 5 Bit Serial Digital Attenuator</td>
</tr>
<tr>
<td>HRF-AT4520</td>
<td>31.0 dB, DC-4 GHz, 5 Bit Parallel Digital Attenuator</td>
</tr>
<tr>
<td>HRF-AT4521</td>
<td>31.0 dB, DC-2.5 GHz, 5 Bit Serial Digital Attenuator</td>
</tr>
<tr>
<td>HRF-AT4610</td>
<td>31.5 dB, DC-4 GHz, 6 Bit Parallel Digital Attenuator</td>
</tr>
<tr>
<td>HRF-AT4611</td>
<td>31.5 dB, DC-4 GHz, 6 Bit Serial Digital Attenuator</td>
</tr>
</tbody>
</table>

**APPLICATION SUMMARY**

**Single and Dual Power Supply Options (P1dB)** This device is designed to allow the choice of using either a single (VDD = +5 volts, and VSS = Ground) or dual voltage supply (VDD = +5 volts, and VSS = negative supply up to –5 volts). As noted on the electrical specification, the P1dB compression point is extended in the latter case by 7 dB to 10 dB proportionally to the negative supply value. Very little current is required by the VSS negative supply pin (µamps). CMOS swings between VDD and ground are maintained for all digital interfaces. RF inputs can be DC coupled, swinging around ground.

**DC RF Interface** This device is designed for DC coupling of the RF swing around ground. No blocking caps are needed so the device is truly DC operational. AC coupling is allowed and could be used to block non-ground centered signals. See AN315 for AC coupling configurations. In the AC case, the cap value determines the low frequency cutoff.

**Package Related Optimization** The 50-ohm RFin/RFout conductor paths should be maintained within close proximity of the package. A ground plane for ground pins and the RF backside ground plate should be employed. The low inductance ground path of the backside ground plate is required for rated performance.

**TYPICAL DIGITAL CONTROL CIRCUITRY**

**Attenuation Accuracy** This family of attenuator products has state of the art attenuation accuracy across the attenuation range. This accuracy is also maintained across the frequency band, and is unmatched within the industry.

**Electrostatic Discharge (ESD) Protection** RF circuits are traditionally difficult to protect without severely impacting performance. The integration capabilities of SOI technology allow the more ESD sensitive nodes to be kept internal to the chip, where they can be protected by the digital interface circuitry. RFin/RFout ports cannot be protected as effectively, therefore they should be handled following standard ESD procedures.

**ADDITIONAL INFORMATION**

In addition to standard attenuator and switch products, Honeywell also provides foundry, design, package and test services. Honeywell designers can also convert GaAs-based designs into CMOS SOI-based devices.

Honeywell reserves the right to make changes to improve reliability, function or design. Honeywell does not assume any liability arising out of the application or use of any products or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.