SOI CMOS Technology for RF System-on-Chip Applications

CMOS technology is one of the most promising choices for RF applications. Its highly integrated nature provides true RF system-on-chip integration. Silicon-on-insulator (SOI) CMOS offers specific additional design advantages that include a significant reduction in cross-talk between RF and digital circuits on the same die and easy integration of high quality passive elements. Basic RF building blocks through 6 GHz have been verified with a 0.35 µm production-ready SOI CMOS technology.

Gallium arsenide (GaAs) has been used extensively for 2 to 6 GHz RF applications due to its intrinsically higher speed. Whenever cost and integration are important technology selection criteria, CMOS is an excellent choice. This is especially true with the advance in CMOS technology, where an $f_t$ beyond 140 GHz is readily demonstrated. Recently, a single chip, 2.4 GHz transceiver for Bluetooth application has been successfully demonstrated with a deep sub-micron CMOS technology, and 900 MHz Industrial, Scientific and Medical (ISM) band transceivers with a direct microcontroller interface have been fabricated. The recent announcement of a single chip, 5 GHz wireless local area network (WLAN) further illustrates the point that CMOS is a viable solution in complicated RF systems. The minimum noise figure, which is an important characteristic in RF front-end design, has also been improved with scaled CMOS. Noise figures as low as 0.2 dB have been reported with proper device layout.

Low power consumption is particularly important in mobile communications due to limited battery life. One approach to meeting this challenge is to create a reduced power RF system-on-chip that contains digital, analog and RF portions of the design on the same die. SOI CMOS meets these requirements due to its reduced parasitic capacitance. The presence of the buried oxide layer not only reduces the junction capacitance but also offers the flexibility of using a high resistivity substrate to reduce the substrate-related RF loss. Microstrip losses as low as 0.03 dB/mm have been realized on high resistivity substrates at 2 GHz compared with 0.1 dB/mm on standard substrates. In addition, improved passive device performance (resistor, capacitor and inductor) over frequency has also been demonstrated on SOI substrates.

Another key concern with highly integrated RF/mixed mode circuit design is how to eliminate the cross-talk between high frequency RF and digital, mixed signal devices on the same die.
die. This can be drastically reduced by using fully oxide-isolated SOI CMOS technology. Complete oxide isolation of the active devices from the substrate eliminates the substrate current injection path. In this article, a review of the current advances in RF SOI CMOS is provided.

SOI TECHNOLOGY

SOI substrates have been fabricated by either oxygen implant/anneal (SIMOX) or bond/etch back (BESOI) techniques. Both have gained acceptance in the market place. Anticipated wafer volume is in the range of 500,000 wafers per year ramping to 10 million per year by 2005. Recently, the two largest SIMOX and BESOI suppliers have formed an alliance with major commercial silicon wafer suppliers to further secure the needed wafer capacity. This milestone illustrates the general acceptance of SOI as a viable technology choice. Large volume production is the only way to ensure continuous price reduction and quality improvement. This is where SOI has a significant advantage over other insulated materials such as silicon-on-sapphire (SOS). Companies such as IBM, Honeywell, AMD, Motorola, Samsung, Matsushita, XFAB and many others are actively producing SOI-based integrated circuits.

Today, RF SOI CMOS-based products operate in the 2 to 10 GHz range without compromising RF performance. As early as 1994, SEMATECH completed an analysis of SOI and bulk CMOS technology that concluded that SOI has the potential to be a lower cost solution because the simpler well/isolation process requires fewer processing steps, thus lowering manufacturing cost. In addition, the study revealed, a higher die leverage, due to improved isolation, yields more good die per wafer and higher performance results from the elimination of substrate capacitances. Table 1 summarizes SEMATECH's original work with updates from some recent publications. Even though the comparison was done with digital SRAM in mind, its conclusion still applies to mixed mode technology.

A cross-section of a multi-layer metal SOI device is shown in Figure 1. A silicon thickness ranging from 50 to 200 nm has been used to fabricate the transistors. With such a thin-film, source and drain junction/depletion width of the MOS transistors can be easily bottomed to the buried oxide, thus reducing the junction capacitance. Combined with the fact that power consumption is directly proportional to the capacitance (power = CV²), SOI technology is playing an increasingly important role in low power mobile application. A typical performance comparison between bulk and SOI technologies is shown in Figure 2.

SUBSTRATE CROSS-TALK REDUCTION

To integrate an RF system-on-chip, it is important to have proper device isolation in the gigahertz frequency range. SOI technology provides the proper device isolation because complete oxide isolation between devices essentially cuts off all direct paths of substrate injection noise and a near intrinsic substrate further reduces the capacitive coupling through the substrate. Complete oxide isolation is impossible to form with bulk CMOS or bipolar technology. To overcome this problem, multiple substrate contacts with large guard band and/or deep trench isolation to reduce the substrate injection current can be used. Either approach suffers a negative impact on density (large guard band) or higher fabrication cost (complex processing of deep trench isolation structures).

As pointed out earlier, the buried oxide layer offers a complete isolation between the active device region and the bulk substrate. This provides an additional degree of freedom in selecting the high resistivity substrate. Using a near intrinsic substrate to reduce the capacitive coupling is impossible for bulk technology due to latch up concerns.
**Inductor Loss Reduction**

*Figure 4* shows the estimated inductor Q vs. frequency for SOI technology. Substrate resistivity plays a key role in determining the inductor Q at high frequencies. Recently, a simple inductor model has been proposed where the roll-off of the Q value at high frequency is dominated by the substrate loss. This can easily be improved by using a high resistivity SOI substrate. A Q of approximately 10 at 5 GHz has been achieved with a simple two layer standard metal process instead of the costly five or six layer thick metal required by the advanced CMOS processes. This is an important attribute of the SOI technology, since not all the RF system-on-chip requires a five or six layer metal interconnect process. One side benefit, of course, is the reduction of the cycle time to manufacture the products.

**Resistor/Capacitor Loss Reduction**

An improvement in resistor performance is also observed on SOI. Comparing a 400 Ω polysilicon resistor, SOI behaves close to the ideal resistor through 18 GHz; bulk resistor, however, suffers from substrate coupling and degrades at frequencies as low as 5 GHz, as shown in *Figure 5*. A similar improvement in capacitor performance is also observed at high frequencies. Since passive elements such as inductors, resistors and capacitors all play a very important role in RF front-end design, high resistivity SOI offers an obvious performance advantage over bulk technology.

**Noise Figure/PAE Improvement**

Gate-degenerated topology is widely used for low noise amplifier (LNA) designs in RF applications. The input inductor, which is directly connected to the gate, could introduce a substantially large amount of capacitive coupling to the substrate, thus degrading both f<sub>I</sub> and noise figure (NF) directly. At least 0.5 dB NF improvement over bulk CMOS has been reported at 2.5 GHz by using the SOI process with a high resistivity substrate.

**SOI CMOS INTEGRATION CAPABILITY**

Since SOI CMOS is a silicon-based technology, a high level of integration can be obtained. An example is shown in *Figure 6*, where a six-bit digital attenuator is integrated with a sophisticated control logic. With early 0.8 μm RF SOI technology, this product has demonstrated good performance characteristics from 300 MHz to more than 1 GHz and is usable to 2 GHz. A variety of integration and control capabilities is also shown. Some of the key advantages of SOI CMOS are the high performance and the ability to integrate passive elements such as resistors, capacitors and inductors.

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**TECHNICAL FEATURE**

![Fig. 3 Pad-to-pad isolation comparison between bulk and SOI devices at 160 μm separation.](image)

![Fig. 4 Inductor Q vs. frequency.](image)

![Fig. 5 Substrate-related RF loss showing a significant reduction in the 400 Ω polysilicon resistor example.](image)

![Fig. 6 An example of a highly integrated six-bit attenuator.](image)

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**TABLE II**

**MICROSTRIP LOSS REDUCTION THROUGH HIGH RESISTIVITY SOI SUBSTRATE**

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Resistivity (Ω-cm)</th>
<th>Loss (dB/mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semi-insulated (GaAs compatible)</td>
<td>10⁶</td>
<td>0.03</td>
</tr>
<tr>
<td>Low resistivity</td>
<td>50</td>
<td>0.54</td>
</tr>
<tr>
<td>High resistivity</td>
<td>10³</td>
<td>0.05</td>
</tr>
</tbody>
</table>

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A pad-to-pad isolation measurement up to 10 GHz is shown in *Figure 3*, where SOI shows a near 30 to 40 dB improvement.

**SUBSTRATE LOSS REDUCTION**

**Microstrip Loss Reduction**

In addition to the above-mentioned cross-talk reduction, a high resistivity substrate further reduces the microstrip loss at high frequency. Since microstrip is widely used for impedance matching, it is important to address the substrate loss issue. Recent studies have shown that on a substrate with a resistivity of 1 kΩ-cm, the loss of a microstrip line at 2 GHz is only 0.05 dB/mm compared with 0.55 dB/mm on a typical 50 Ω-cm substrate. A factor of 18 improvement is easily achievable on SOI substrate. This comparison is summarized in *Table 2*.

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**Figure 4** shows the estimated inductor Q vs. frequency for SOI technology. Substrate resistivity plays a key role in determining the inductor Q at high frequencies. Recently, a simple inductor model has been proposed where the roll-off of the Q value at high frequency is dominated by the substrate loss. This can easily be improved by using a high resistivity SOI substrate. A Q of approximately 10 at 5 GHz has been achieved with a simple two layer standard metal process instead of the costly five or six layer thick metal required by the advanced CMOS processes. This is an important attribute of the SOI technology, since not all the RF system-on-chip requires a five or six layer metal interconnect process. One side benefit, of course, is the reduction of the cycle time to manufacture the products.
able gain amplifier with 22 dB of gain and 60 dB attenuation in 0.5 dB steps has also been realized with SOI CMOS technology. This frequency range can easily be extended to 4 GHz with a 0.35 µm SOI CMOS technology.

CONCLUSION

SOI CMOS is a cost-effective, viable technology for RF system-on-chip integration up to 10 GHz due to its ability to achieve higher levels of device integration without compromising RF performance. Reduction in cross-talk and easy integration of passive elements are key attributes to SOI CMOS technology.

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References


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