

# HX422R

## Quad RS422 Differential Line Receiver Radiation Hardened 3.3V SOI CMOS

### Features

- Four Independent Receivers
- Rad Hard: >300k Rad(Si) Total Dose
- Single +3.3 V Analog Supply
- Common Receiver Enable Control
- Tristate Outputs
- Temperature Range: -55°C to 125°C
- Generally Compatible to TIA/EIA-422-B
- Built in Hysteresis
- 10mA Output Drive
- Maximum Data Rate: 20Mb/s

### Mixed Signal Rad Hard Process

The HX422R is fabricated on space qualified SOI CMOS process. High-speed precision analog circuits are now combined with high-density logic circuits that can reliably withstand the harshest environments.

### Low Power

The HX422R dissipates less than 200mW with all outputs toggling at 10MHz data rate.

### Common Receiver Enable Control (EN, EN\*)

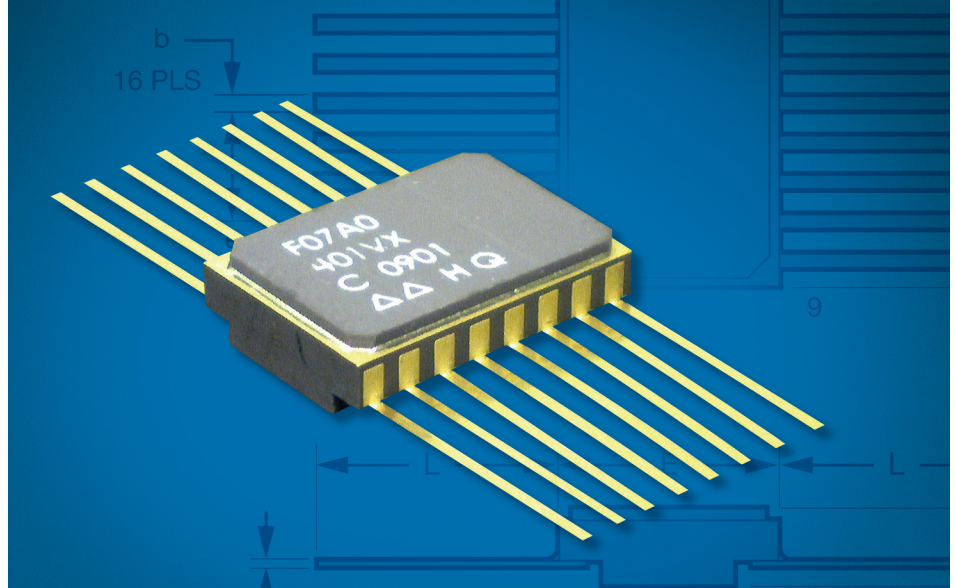
The EN and EN\* inputs allow the user to put the digital outputs into high impedance three-state mode.

### Dual Power Supply Capability

The HX422R uses a single +3.3V power supply simplifying system power supply design.

### Space Qualified Package

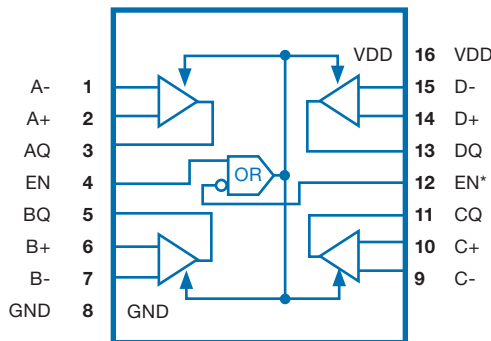
The HX422R is packaged in a 16 lead ceramic flat pack.



The HX422R is a radiation hardened Silicon On Insulator (SOI) CMOS quad differential line receiver designed to meet the standard RS422 requirements and digital data transmission over balanced lines. It features four independent receivers with a common receiver enable

control and high impedance outputs. The HX422R has a maximum operating frequency of 20Mb/s. The circuit has built in hysteresis to improve noise margin and output stability for slow changing input signals.

### Package Pinout



### Truth Table

| EN | EN* | V <sub>IN(DIFF)</sub> | Q |
|----|-----|-----------------------|---|
| L  | H   | X                     | Z |
| H  | X   | <-200 mV              | L |
| X  | L   | <-200 mV              | L |
| H  | X   | >+200 mV              | H |
| X  | L   | >+200 mV              | H |

### Signal Definition

| Signal         | Description   |
|----------------|---|
| A+, A- B+, B-  | Differential Data Input signals   |
| C+, C- D+, D-  | Differential Data Input signals   |
| AQ, BQ, CQ, DQ | Output signals, CMOS levels   |
| EN, EN*        | Output Enable Control pins. The combination of EN = L and EN* = H will put the outputs into the high impedance state. All other combinations of EN and EN* will allow data through the drivers. |

## Recommended Operating Conditions

| Parameter                                      | Symbol           | Conditions           | Limits |           | Units |
|--|------------------|----------------------|--------|-----------|-------|
|  |                  |                      | Min    | Max       |       |
| Supply Voltage                                 | $V_{DD}$         |                      | 3.0    | 3.6       | V     |
| Input Voltage A+/-, B+/-, C+/-, D+/-           | $V_{IN(DIFF)}$   |                      | -7     | 7         | V     |
| Input Voltage (E+, E-)                         | $V_{IN(Enable)}$ |                      | 0      | VDD       | V     |
| Input Common Mode Range A+/-, B+/-, C+/-, D+/- | VCM              |                      | -6     | +6        | V     |
| Differential Input Voltage                     | $V_{DIFF}$       |                      | -5     | +5        | V     |
| High Level Input Voltage (E+, E-)              | $V_{IH}$         | VDD = 3.0 V to 3.6 V | 0.7VDD |           | V     |
| Low Level Input Voltage (E+, E-)               | $V_{IL}$         | VDD = 3.0 V to 3.6 V |        | 0.3VDD    | V     |
| Output Voltage                                 | VO               |                      | -0.3   | VDD + 0.3 | V     |
| Case Operating Temperature                     | $T_C$            |                      | -55    | +125      | °C    |

## Absolute Maximum Ratings (1)(2)

| Parameter                                | Symbol         | Conditions         | Limits |                | Units |
|--|----------------|--------------------|--------|----------------|-------|
|  |                |                    | Min    | Max            |       |
| Supply Voltage                           | $V_{DD}$       | —                  | -0.5   | +6.5           | V     |
| DC Input Voltage (EN, EN*)               | $V_{IN}$       |                    | -0.5   | VDD + 0.5      | V     |
| Common Mode Range                        | $V_{CM}$       | —                  | -7     | +7             | V     |
| Input Voltage A+/-, B+/-, C+/-, D+/-     | $V_{IN(DIFF)}$ | —                  | -8     | +8             | V     |
| Differential Input Voltage               | $V_{DIFF}$     |                    | -6.5   | +6.5           | V     |
| Receiver Output Voltage (AQ, BQ, CQ, DQ) | VO             | —                  | -0.5   | $V_{DD} + 0.5$ | V     |
| Input Diode Clamp Current                | $I_{IK}$       |                    | -180   | +180           | mA    |
| Output Short Circuit Current             | $I_{OS}$       | 1 second, 1 output | 15     | 120            | mA    |
| Receiver Output Current                  | IO             | —                  | -20    | +20            | mA    |
| Storage Temperature                      | $T_{STG}$      |                    | -65    | +150           | °C    |
| Thermal Resistance, Junction to Case     | $\theta_{JC}$  |                    |        | 16.5           | °C/W  |
| Junction Temperature                     | $T_J$          | —                  | —      | +175           | °C    |
| Lead Temperature (soldering, 5 seconds)  | $T_{LMAX}$     | —                  | —      | +300           | °C    |
| ESD (HBM)                                | —              | —                  | 2000   | —              | V     |

(1) Stresses above absolute maximum ratings may cause damage to the device.

(2) The input overshoot and undershoot voltage can exceed voltage limits provided that the input and output clamp currents are not exceeded.

## Radiation Hardness Ratings

| Parameter                 | Limits                  | Units             | Test Conditions                           |
|---------------------------|-------------------------|-------------------|---|
| Total Dose (3)            | $\geq 300$              | krad(Si)          | VDD = Maximum                             |
| Transient Dose Rate Upset | $\geq 1 \times 10^9$    | rad(Si)/s         | PW = 20ns, 3 $\mu$ s X-ray, VDD = Minimum |
| Dose Rate Survivability   | $\geq 1 \times 10^{12}$ | rad(Si)/s         | PW = 20ns, 3 $\mu$ s X-ray, VDD = Maximum |
| Neutron Fluence           | $\geq 1 \times 10^{14}$ | N/cm <sup>2</sup> | 1MeV equivalent energy, Unbiased          |

(1) Ambient temperature 25°C unless otherwise specified.

(2) Device will not latch up due to any of the specified radiation exposure conditions.

## Radiation Performance

### Total Ionizing Radiation Dose

The device will meet all stated functional and electrical specifications after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications, post rebound (based on extrapolation), after an operational period of 15 years. Total dose hardness is assured by wafer level testing of process monitor transistors using 10 KeV X-ray. Parameter correlations have been made between 10 KeV X-rays applied at a dose rate of  $5 \times 10^5$  rad(SiO<sub>2</sub>)/min at T= 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

### Transient Pulse Ionizing Radiation

The HMXMUX01 will meet any functional or electrical specification after exposure to a radiation pulse up to the transient dose rate survivability specification, when applied under recommended operating conditions. Note that the current conducted during

the pulse by the MUX inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

### Neutron Radiation

The device will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions.

### Latchup and Snapback

The Analog Multiplexer will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SOI substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. Sufficient transistor body tie connections to the p- and n-channel substrates are made to ensure no source/drain snapback occurs.

## ESD (Electrostatic Discharge) Sensitive

The HX422R is ESD rated as Class 2 per ANSI/ESD S20.20. Proper ESD precautions should be taken to avoid degradation or damage to the device.

## Electrical Requirements (1)(2)(3)

| Parameter  | Symbols            | Conditions   | Min   | Limits Max | Units |
|--|--------------------|--|-------|------------|-------|
| Supply Current                                       |                    | V <sub>DD</sub> = 3.6 V, all outputs toggling                                    |       |            | mA    |
|  | I <sub>DDOP1</sub> | 2Mb/s  | —     | 40         |       |
|  | I <sub>DDOP3</sub> | 10 Mb/s  | —     | 60         |       |
| Differential Line Input Voltage (2)                  | V <sub>TH6</sub>   | V <sub>CM</sub> = +6V, V <sub>DD</sub> =3.0V                                     | -200  | 200        | mV    |
|  | V <sub>TH0</sub>   | V <sub>CM</sub> = 0V, V <sub>DD</sub> =3.0V                                      | -200  | 200        |       |
|  | V <sub>THM6</sub>  | V <sub>CM</sub> = -6V, V <sub>DD</sub> =3.0V                                     | -200  | 200        |       |
| Differential Line Input Threshold Hysteresis (2) (4) | V <sub>HY</sub>    | V <sub>CM</sub> = 0  | 5     | 100        | mV    |
| Input Resistance (Line pins) (2) (4)                 | R <sub>IN6</sub>   | V <sub>CM</sub> = +6V  | 6k    | 15k        | Ohms  |
|  | R <sub>IN0</sub>   | V <sub>CM</sub> = 0  | 6k    | 15k        |       |
|  | R <sub>INM6</sub>  | V <sub>CM</sub> = -6V  | 6k    | 15k        |       |
| Input Current (Line pins) (2)                        | I <sub>IH1</sub>   | V <sub>CM</sub> = +6V  | —     | 1000       | μA    |
|  | I <sub>IL1</sub>   | V <sub>CM</sub> = -6V  | -1300 | —          |       |
| Input Threshold (E+, E-) (3)                         | V <sub>IL</sub>    | V <sub>DD</sub> = 3.0 V  | 0.9   | —          | V     |
| Input Threshold (E+, E-) (3)                         | V <sub>IH</sub>    | V <sub>DD</sub> = 3.6 V  | —     | 2.52       | V     |
| Input Current (Enable) (3)                           | I <sub>IH2</sub>   | V <sub>DD</sub> = 3.6 V, V <sub>IN</sub> = 3.6V or 0V                            | -10   | 10         | μA    |
|  | I <sub>IL2</sub>   |  |       |            |       |
| Output Tristate Current                              | I <sub>OZL</sub>   | V <sub>DD</sub> = 3.6 V, outputs disabled, tester force 0 V (I <sub>OZ_L</sub> ) | -10   | 10         | μA    |
|  | I <sub>OZH</sub>   | or 3.6 V (I <sub>OZ_H</sub> ) on output pins                                     |       |            |       |
| Output High Voltage                                  | V <sub>OH</sub>    | I <sub>OH</sub> = -10 mA, V <sub>DD</sub> = 3.0V                                 | 2.5   | —          | V     |
| Output Low Voltage                                   | V <sub>OL</sub>    | I <sub>OL</sub> = 10 mA V <sub>DD</sub> = 3.0 V                                  | —     | 0.5        | V     |
| Input Capacitance Diff Inputs (2) (4)                | C <sub>I</sub>     |  |       | 12         | pF    |
| Output Capacitance CMOS Outputs (4)                  | C <sub>O</sub>     |  |       | 15         | pF    |

(1) Test conditions shall be as follows: 3.0 V ≤ V<sub>DD</sub> ≤ 3.6 V, -55°C ≤ T<sub>C</sub> ≤ +125°C, V<sub>SS</sub> = 0 V

(2) Differential inputs refer to A-, A+, B-, B+, C-, C+, D-, D+.

(3) E+, E- are the Enable pins.

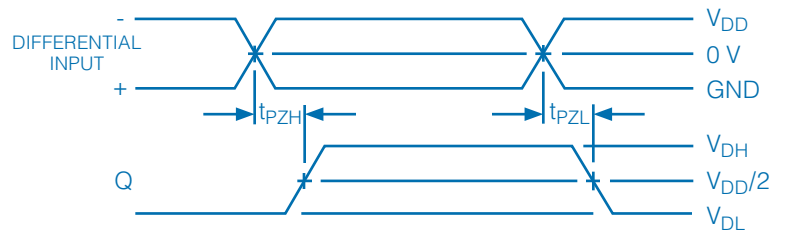
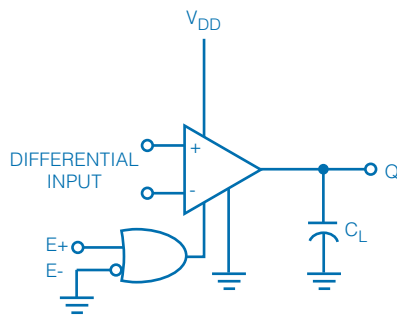
(4) Guaranteed but not tested.

## Timing Parameters

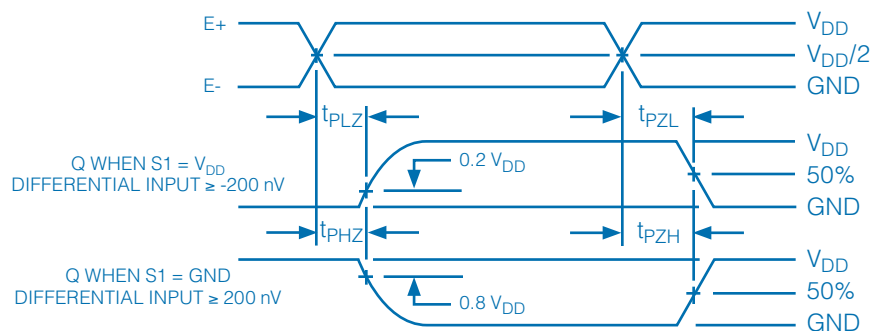
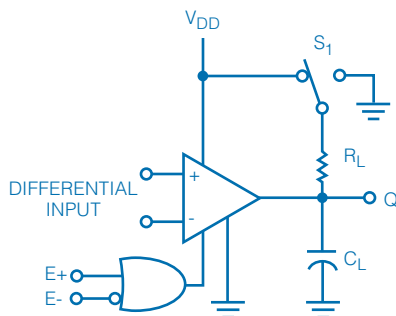
| Parameter                                  | Symbol      | Condition   | Limits |     | Units |
|--|-------------|---|--------|-----|-------|
|  |             |   | Min    | Max |       |
| Differential Propagation Delay High to Low | $T_{PHL1}$  | $V_{DD} = 3.0, 3.6\text{ V}$ $CL = 15\text{ pF}$<br>$VDIFF = 500\text{ mV}$ | 0      | 54  | nS    |
|  | $T_{PHL2}$  | $VDIFF = 1000\text{ mV}$  | 0      | 45  | nS    |
| Differential Propagation Delay Low to High | $T_{PLH1}$  | $V_{DD} = 3.0, 3.6\text{ V}$ $CL = 15\text{ pF}$<br>$VDIFF = 500\text{ mV}$ | 0      | 54  | nS    |
|  | $T_{PLH2}$  | $VDIFF = 1000\text{ mV}$  | 0      | 45  | nS    |
| Disable Time High to Z                     | $T_{PHZ}$   | $V_{DD} = 3.0, 3.6\text{ V}$ $CL = 15\text{ pF}$                            | 0      | 25  | nS    |
| Disable Time Low to Z                      | $T_{PLZ}$   | $I_{OH} = -10\text{ mA}$  | 0      | 25  | nS    |
| Enable Time Z to Low                       | $T_{PZL}$   | $I_{OL} = +10\text{ mA}$  | 2.5    | 25  | nS    |
| Enable Time to High                        | $T_{PZH}$   |   | 2.5    | 25  | nS    |
| Maximum Data Rate                          | $F_{DATA1}$ | $V_{DD} = 3.0, 3.6\text{ V}$<br>$VDIFF = 200\text{ mV}$                     | 10     |     | Mb/s  |
|  | $F_{DATA2}$ | $VDIFF = 1000\text{ mV}$  | 20     |     | Mb/s  |
| Maximum Operating Frequency                | $F_{MAX1}$  | $V_{DD} = 3.0, 3.6\text{ V}$<br>$VDIFF = 200\text{ mV}$                     | 5      |     | MHz   |
|  | $F_{MAX2}$  | $VDIFF = 1000\text{ mV}$  | 10     |     | MHz   |

## Test Circuits And Diagrams

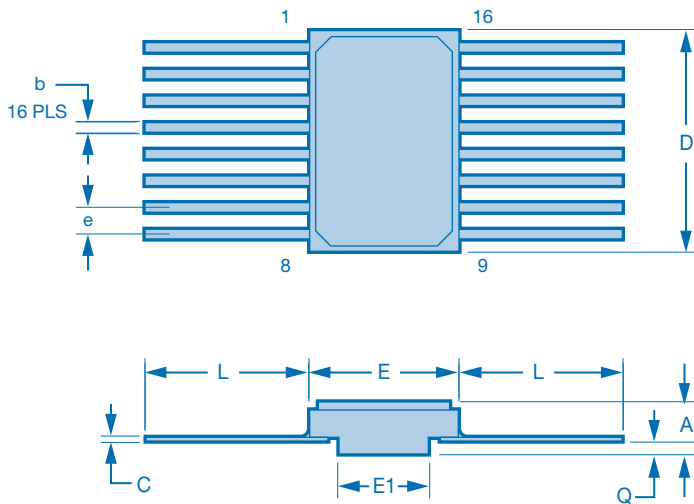
### $T_{PLH}$ and $T_{PHL}$ Test Circuit and Waveform



### $T_{PHZ}$ , $T_{PZH}$ , $T_{PLZ}$ , and $T_{PZL}$ Test Circuit and Waveform



## Package Outline Dimensions



| Symbol | Dimensions - Inches |      | Dimensions - Millimeters |       |
|--------|---------------------|------|--------------------------|-------|
|        | Min                 | Max  | Min                      | Max   |
| A      | .101                | .125 | 2.57                     | 3.18  |
| b      | .015                | .019 | 0.38                     | 0.48  |
| c      | .004                | .007 | 0.11                     | 0.18  |
| D      | .392                | .408 | 9.96                     | 10.36 |
| e      | .047                | .053 | 1.20                     | 1.34  |
| E      | .274                | .286 | 6.96                     | 7.26  |
| E1     | .185                | .196 | 4.70                     | 4.96  |
| L      | .320                | .360 | 8.13                     | 9.14  |
| Q      | .022                | .032 | 0.56                     | 0.82  |

## Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the S150 process technology. This approach includes adhering to Honeywell's General Manufacturing Standards for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDDB, hot carriers, negative bias temperature instability, radiation)
- Utilizing a structured and controlled design process
- A statistically controlled wafer fabrication process with a continuous defect reduction process
- Individual wafer lot acceptance through process monitor testing (includes radiation testing)
- The use of characterized and qualified packages
- A thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

## Qualification and Screening

The SOI CMOS technology is qualified by Honeywell after meeting the criteria of the General Manufacturing Standards and is also QML Qualified. This qualification is the culmination of years of development, testing, documentation, and on-going process control.

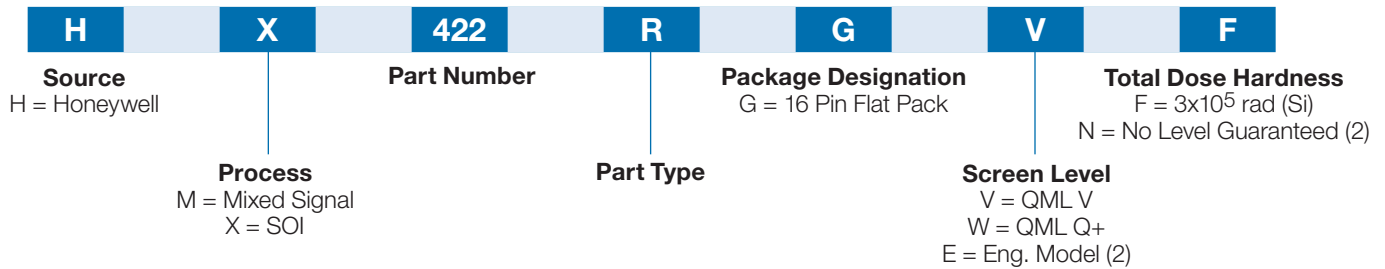
The test flow includes screening units with the defined flow (Class V and Q+) and the appropriate periodic or lot conformance testing (Groups B, C, D, and E). Both the process and the products are subject to period or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests, respectively, as defined by Honeywell's Quality Management Plan.

Honeywell delivers products that are screened to two levels including Engineering Models and Flight Units. EMs are available with limited screening for prototype development and evaluation testing.

|         |  |
|---------|--|
| Group A | Final Lot Acceptance Electrical Tests  |
| Group B | Mechanical – Dimensions, Bond Strength, Solvents, Die Shear, Solderability, Lead Integrity, Seal, Acceleration                               |
| Group C | Life Tests – 1000 hours at 125°C or equivalent   |
| Group D | Package related mechanical tests – Shock, Vibration, Accel, Salt, Seal, Lead Finish Adhesion, Lid Torque, Thermal Shock, Moisture Resistance |
| Group E | Radiation Tests  |

(1) Testing performed by package supplier.

## Ordering Information



(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 for further information.

(2) Engineering Device Description: Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation guaranteed.

## Standard Microcircuit Drawing

The HX422R can be ordered under the SMD drawing 5962-07A04.

## QCI Testing (1)

| Classification | QCI Testing  |
|----------------|--|
| QML Q+         | No lot specific testing performed. (2)                                     |
| QML V          | Lot specific testing required in accordance with MIL-PRF-38535 Appendix B. |

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell Quality Management Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.

(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

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## Find out more

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