HXLVDSD

Honeywell

Quad LVDS Differential Line Driver Radiation Hardened 3.3V SOI CMOS

Features

- Four Independent Drivers
- Rad Hard: >300k Rad(Si) Total Dose
- Single +3.3 V Supply
- Common Driver Enable Control
- Tristate Outputs
- Temperature Range: -55°C to 125°C
- Minimum Differential Output Signal: 250mV
- Maximum Operating Frequency > 100MHz

- **Low Power**

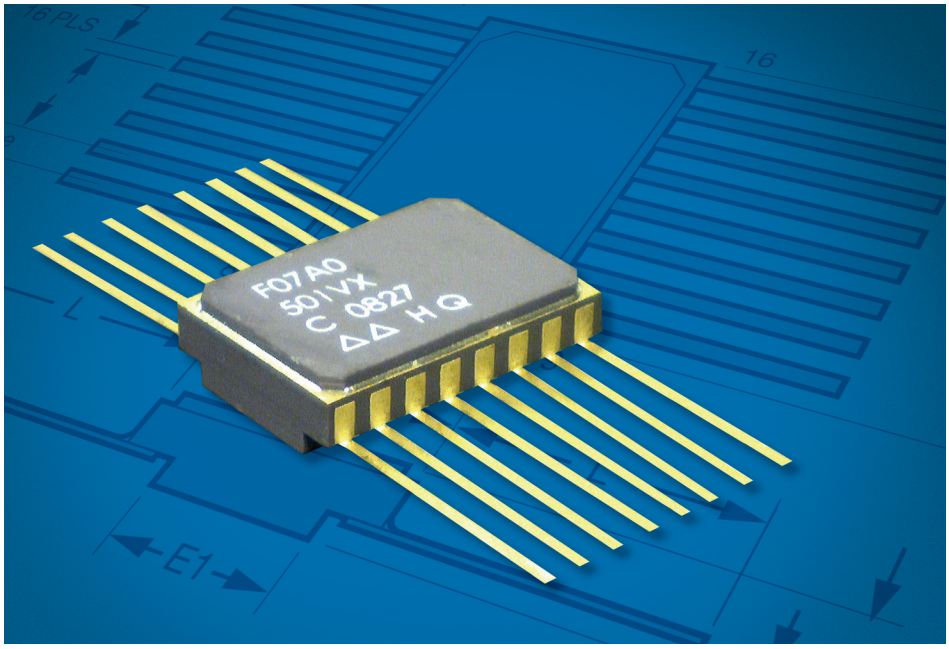
  The HXLVDSD dissipates less than 300mW with all outputs toggling at a data rate of 100MHz.

- **Common Receiver Enable Control (EN, EN*)**

  The EN and EN* inputs allow the user to put the digital outputs into high impedance tri-state mode.

- **Space Qualified Package**

  The HXLVDSD is packaged in a 16 lead ceramic flat pack.

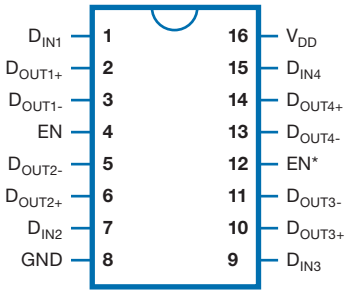


The HXLVDSD is a radiation hardened quad differential line driver with tristate outputs. It features four independent drivers with a common driver enable control and high impedance outputs. The HXLVDSD along with the HXLVDSR provide an alternative to high power devices for high speed point to point interface applications.

The HXLVDSD is a radiation hardened SOI-IV Silicon On Insulator (SOI) process with very low power consumption.

The input of the HXLVDSD allows for easy interfacing to space and military imaging, sensor, and communications systems.

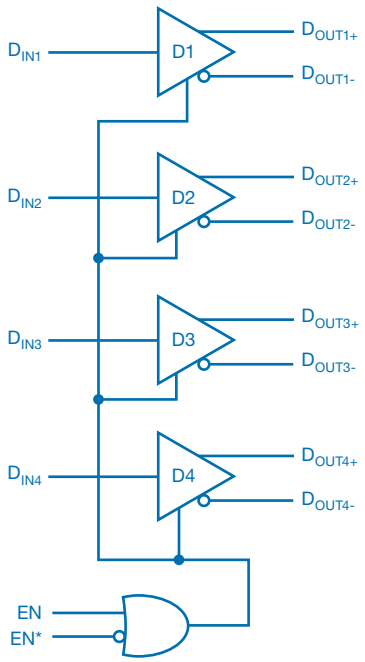
Pin Diagram



Pin Description

Pin	Symbol	Signal Type	Buffer Definition
1	D_{IN1}	I	CMOS
2	D_{OUT1+}	O	LVDS
3	D_{OUT1-}	O	LVDS
4	EN	I	CMOS
5	D_{OUT2-}	O	LVDS
6	D_{OUT2+}	O	LVDS
7	D_{IN2}	I	CMOS
8	GND	GND	GND/VSS = 0V
9	D_{IN3}	I	CMOS
10	D_{OUT3+}	O	LVDS
11	D_{OUT3-}	O	LVDS
12	EN*	I	CMOS
13	D_{OUT4-}	O	LVDS
14	D_{OUT4+}	O	LVDS
15	D_{IN4}	I	CMOS
16	V_{DD}	PWR	V_{DD}

Block Diagram



Truth Table

ENABLES		INPUT	DIFF OUTPUT
EN	EN*	DIN	DOUT+ - DOUT-
L	H	X	Z
H	X	L	L
X	L	L	L
H	X	H	H
X	L	H	H

Signal Definition

Signal	Definition
EN - EN*	EN and EN* are the common enable control signals. As shown in the truth table, the combination of EN = L and EN* = H puts the outputs into the high impedance state. The outputs are enabled for all other combinations of EN and EN*.
D_{IN1} - D_{IN4}	Data Inputs
D_{OUT} - D_{OUT}	Differential Outputs

The HXLVDSD is a radiation hardened quad differential line driver designed for applications requiring low power dissipation and high data rates. The HXLVDSD accepts 3.3V CMOS input voltage levels and translates them into low voltage differential (LVDS) output levels. The EN and EN* inputs allow active Low or active High control of the tristate outputs. The enable signals are common to all four drivers. The dual enable scheme allows for flexibility in turning devices on or off.

Absolute Maximum Ratings (1)

Parameter	Symbol	Conditions	Limits		Units
			Min	Max	
Supply Voltage	V_{DD}	—	-0.5	+4.6	V
DC Input Voltage	V_{IN}	—	-0.5	V_{DD}+0.5	V
DC Output Voltage	V_{OUT+}, V_{OUT-}	—	-0.5	V_{DD}+0.5	V
Enable Input Voltage	(EN, EN*)	—	-0.5	V_{DD}+0.5	V
Input Diode Clamp Current	I_{IK}	V_{IN} < 0-V_{TH_diode} or V_{IN} > V_{DD}+$V_{TH\ diode}$	-42	+42	mA
Short Circuit I High (max) LVDS Output Shorted to Complement Output, (2)	I_{OSH1}	V_{DD} = 3.6 V	-16	—	mA
Short Circuit I Low (max) LVDS Output Shorted to Complement Output, (2)	I_{OSL1}	V_{DD} = 3.6 V	—	+16	mA
Short Circuit I High (max) LVDS Output Shorted to VSS, (2)	I_{OSH2}	V_{DD} = 3.6 V, V_{OUT} = VSS	-27	—	mA
Short Circuit I Low (max) LVDS Output Shorted to VDD, (2)	I_{OSL2}	V_{DD} = 3.6 V, V_{OUT} = V_{DD}	—	+27	mA
Maximum Continuous Current per Output Pin	—	—	-19.5	+19.5	mA
DC Output Current, per Pin	I_O	V_{OUT} = 0 to V_{DD}	-50	+50	mA
Thermal Resistance, Junction to Case	θ_{JC}	—	—	+22.2	°C/W
Storage Temperature Range	T_{STG}	—	-65	+150	°C
Lead Temperature (Soldering, 10 sec.)	T_{LMAX}	—	—	+300	°C
Junction Temperature	T_J	—	—	+175	°C
ESD (HBM)	—	—	2000	—	V

(1) Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.
(2) One output at a time should be shorted and the maximum junction temperature should not be exceeded. It should be tested for a maximum of 1 second.

Recommended Operating Conditions

Parameter	Symbol	Limits		Units
		Min	Max	
Supply Voltage	V_{DD}	+3.0	+3.6	V
Case Temperature	T_C	-55	+125	°C
High Level Input Voltage, VDD = 3.0 V to 3.6 V	V_{IH}	$0.7V_{DD}$	—	V
Low Level Input Voltage, VDD = 3.0 V to 3.6 V	V_{IL}	—	$0.3V_{DD}$	V
Input Voltage	V_{IN}	-0.3	V_{DD} + 0.3	V

Electrical Requirements

Parameter	Symbols	Conditions	Limits		Units
			Min	Max	
Differential Output Voltage Min (LVDS Outputs)	V_{OD1}	V_{DD} = 3.0 V, R_L = 100 ±1% Ω	250	—	mV
Differential Output Voltage Max (LVDS Outputs)	V_{OD2}	V_{DD} = 3.6 V, R_L = 100 ±1% Ω	—	550	mV
Change in Magnitude of VOD1 for Complementary					
Output States (LVDS Outputs), (1)	ΔV_{OD1}	R_L = 100 ±1% Ω	—	50	lmVl
Offset Voltage Min (LVDS Outputs)	V_{OS1}	V_{DD} = 3.0 V, R_L = 100 ±1% Ω	—	1.4	V
Offset Voltage Max (LVDS Outputs)	V_{OS2}	V_{DD} = 3.6 V, R_L = 100 ±1% Ω	1.1	—	V
Change in Magnitude of VOS for Complementary					
Output States (LVDS Outputs), (1)	ΔV_{OS}	R_L = 100 ±1% Ω	—	50	lmVl
Output High Voltage (LVDS Outputs)	V_{OH1}	V_{DD} = 3.0 V, R_L = 100 ±1% Ω	—	1.850	V
Output High Voltage (LVDS Outputs)	V_{OH2}	V_{DD} = 3.6 V, R_L = 100 ±1% Ω	—	1.850	V
Output Low Voltage (LVDS Outputs)	V_{OL1}	V_{DD} = 3.0 V, R_L = 100 ±1% Ω	0.800	—	V
Output Low Voltage (LVDS Outputs)	V_{OL2}	V_{DD} = 3.6 V, R_L = 100 ±1% Ω	0.800	—	V
Input High Voltage (CMOS Inputs)	V_{IH}	For D_{IN}, EN, and EN*, V_{DD} = 3.6 V	—	2.52	V
Input Low Voltage (CMOS Inputs)	V_{IL}	For D_{IN}, EN, and EN*, V_{DD} = 3.0 V	0.9	—	V
Input Current (CMOS Inputs)	I_{IH}	V_{IN} = V_{DD}, for D_{IN}, EN, and EN*, V_{DD} = 3.6 V	-10	+10	µA
	I_{IL}	V_{IN} = GND, for D_{IN}, EN, and EN*, V_{DD} = 3.6 V	-10	+10	
Power-off Leakage	I_{OFF}	V_{OUT} = 2.4V, V_{DD} = GND	-10	+10	µA
Output Power-Down State	I_{OZL}	EN = GND and EN* = V_{DD}, V_{DD} = 3.6 V, VO = 0V	-10	+10	µA
	I_{OZH}	EN = GND and EN* = V_{DD}, V_{DD} = 3.6 V, VO = V_{DD}	-10	+10	
Static Supply Current, Drivers Enabled (all differential outputs are loaded, no toggle at inputs)	I_{DDL}	V_{DD} = 3.6 V, R_L = 100 ±1% Ω, All Channels, D_{IN} = V_{DD} or GND,	—	51	mA
Standby Supply Current, Driver Disabled	I_{DDSB}	V_{DD}=3.6 V, EN = GND, EN* = V_{DD}, Vin=0V	—	5	mA
Dynamic Supply Current, Drivers Enabled	V_{DD} = 3.6 V, All outputs loaded with 100 Ohm loads, all outputs toggling.				
	I_{DDOP1}	1 MHz	—	62	mA
	I_{DDOP2}	10 MHz	—	65	mA
	I_{DDOP3}	50 MHz	—	77	mA
	I_{DDOP4}	100 MHz	—	81	mA

Radiation Hardness Ratings (1)(2)

Parameter	Limits	Units	Test Conditions
Total Dose (3)	≥300	krad(Si)	VDD= Maximum
Transient Dose Rate Upset	≥$1x10^9$	rad(Si)/s	PW = 20ns, 3µs X-ray, VDD = Minimum
Dose Rate Survivability	≥1 $x10^{12}$	rad(Si)/s	PW = 20ns, 3µs X-ray, VDD = Maximum
Neutron Fluence	≥1 $x10^{14}$	N/cm^2	1MeV equivalent energy, Unbiased

(1) Ambient temperature 25°C unless otherwise specified.
(2) Device will not latch up due to any of the specified radiation exposure conditions.

Radiation Performance

Total Ionizing Radiation Dose

The device will meet all stated functional and electrical specifications after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications, post rebound (based on extrapolation), after an operational period of 15 years. Total dose hardness is assured by wafer level testing of process monitor transistors using 10 KeV X-ray. Parameter correlations have been made between 10 KeV X-rays applied at a dose rate of $5x10^5$ rad(SiO_2)/min at T= 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The HXLVDSD will meet any functional or electrical specification after exposure to a radiation pulse up to the transient dose rate survivability specification, when applied under recommended operating conditions. Note that the current conducted during the pulse by the inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The HXLVDSD will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions.

Latchup and Snapback

The HXLVDSD will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions.

Capacitance Parameters (1)

Parameter	Symbols	Conditions	Limits Min	Limits Max	Units
Input Capacitance (CMOS Inputs)	C_I		—	12	pF
Output Capacitance, Package capacitance with respect	C_O		—	17	pF
to ground as seen by the on-chip (LVDS outputs)					

(1) Guaranteed but not tested.

Switching Parameters

Parameter	Symbols	Conditions	Limits Min	Limits Max	Units
Driver output jitter (1) (2)	t_{PWD1}	Data	—	350	ps
Driver output jitter with power supply distortion, (1) (2)	t_{PWD2}	Data	—	400	ps
Driver output jitter (1) (2)	t_{PWD1}	Clock	—	7	ps
Driver output jitter with power supply distortion, (1) (2)	t_{PWD2}	Clock	—	80	ps
Differential Propagation Delay High to Low	t_{PHLD}	R_L = 100 ±1% Ω, C_L = 10 pF	0.8	3.6	ns
Differential Propagation Delay Low to High	t_{PLHD}	R_L = 100 ±1% Ω, C_L = 10 pF	0.8	3.7	ns
Differential Pulse Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$, (1)	t_{SKD}	R_L = 100 ±1% Ω, C_L = 10 pF	0.0	0.5	ns
Differential Channel-to-Channel Skew, (1)	ΔSK_{CC}	R_L = 100 ±1% Ω, C_L = 10 pF	0.0	0.5	ns
Differential Part to Part Skew, (1)	ΔSK_{PP1}	R_L = 100 ±1% Ω, C_L = 10 pF	0.0	1.0	ns
Differential Part to Part Skew, (1)	ΔSK_{PP2}	R_L = 100 ±1% Ω, C_L = 10 pF	0.0	1.3	ns
LVDS Output Rise Time, 20%-80% of signal swing, (1)	t_R	R_L = 100 ±1% Ω, C_L = 10 pF	—	1.5	ns
LVDS Output Fall Time, 20%-80% of signal swing, (1)	t_F	R_L = 100 ±1% Ω, C_L = 10 pF	—	1.5	ns
Disable Time High to Z	t_{PHZ}	R_L = 100 ±1% Ω, C_L = 10 pF		5.0	ns
Disable Time Low to Z	t_{PLZ}	R_L = 100 ±1% Ω, C_L = 10 pF		5.0	ns
Enable Time Z to High	t_{PZH}	R_L = 100 ±1% Ω, C_L = 10 pF	0.8	8.5	ns
Enable Time Z to Low	t_{PZL}	R_L = 100 ±1% Ω, C_L = 10 pF	0.8	7.0	ns
Maximum Operating Frequency	f_{MAX}		100	—	MHz

(1) Guaranteed but not tested by vendor.

(2) Maximum LVDS Driver Jitter performance is guaranteed between -5°C and 125°C case temperature, between 3.0 V and 3.6 V; and pre- and post-radiation.

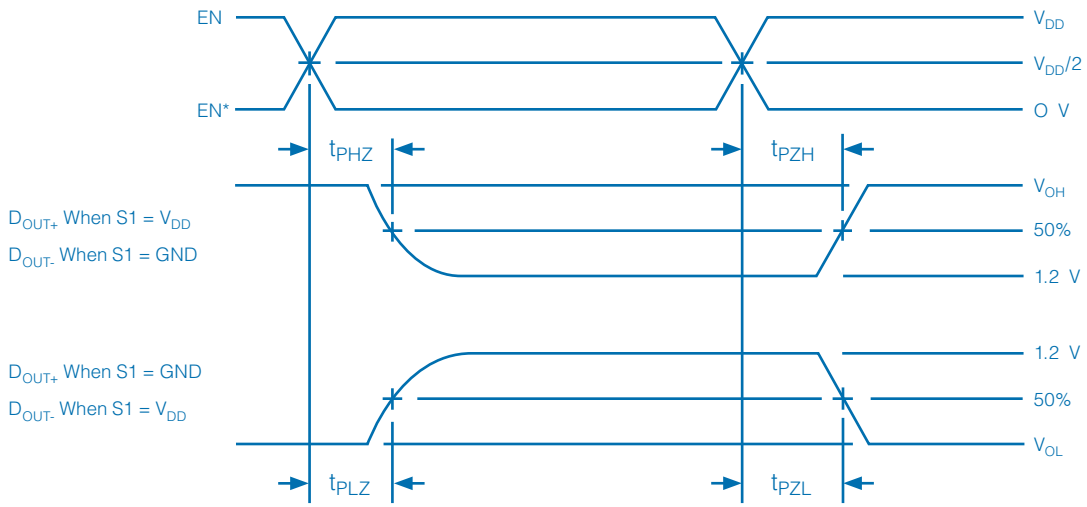
a. Driver CMOS input signal transition time of 1 ns, 10%-to-90% for a 0V-V_{DD} waveform.

b. Driver differential output is terminated with Z_{load} = 100 Ω ± 1% resistor, between (p) and (n) output, and C_{load} = 10 pF from each output to ground.

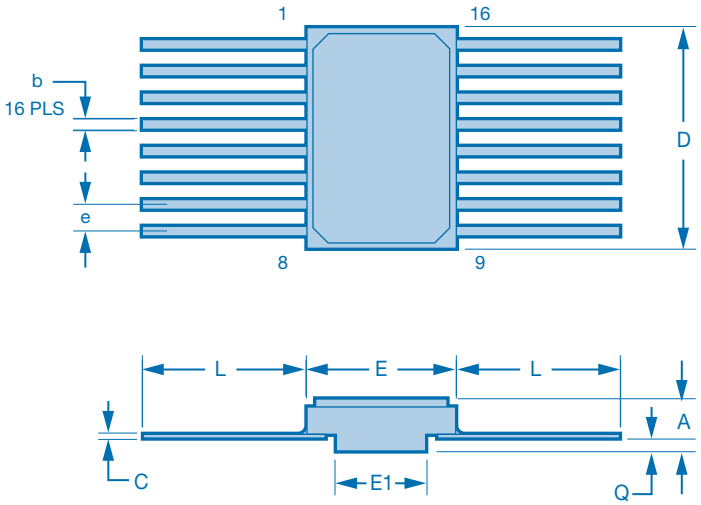
c. For Data jitter measurement, apply a minimum of 250 Pseudo Random Bit Stream (PRBS) bits, at 25 Mbps rate, with no more than 10 consecutive non-transitioning bits in the data stream, at transmitter CMOS input, and measure peak-to-peak data jitter across 100 Ω resistor at LVDS output.

d. For Clock jitter measurement, apply a 50 MHz clock at LVDS driver CMOS input, and measure RMS Time Interval Error (TIE) jitter on rising edge of the LVDS driver output.

Timing Diagram



Package Outline Dimensions



Symbol	Dimensions - Inches Min	Dimensions - Inches Max	Dimensions - Millimeters Min	Dimensions - Millimeters Max
A	.101	.125	2.57	3.18
b	.015	.019	0.38	0.48
c	.004	.007	0.11	0.18
D	.392	.408	9.96	10.36
e	.047	.053	1.20	1.34
E	.274	.286	6.96	7.26
E1	.185	.196	4.70	4.96
L	.320	.360	8.13	9.14
Q	.022	.032	0.56	0.82

Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's General Manufacturing Standards for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, negative bias temperature instability, radiation)
- Utilizing a structured and controlled design process
- A statistically controlled wafer fabrication process with a continuous defect reduction process
- Individual wafer lot acceptance through process monitor testing (includes radiation testing)
- The use of characterized and qualified packages
- A thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

Qualification and Screening

The SOI CMOS technology is qualified by Honeywell after meeting the criteria of the General Manufacturing Standards and is also QML Qualified. This qualification is the culmination of years of development, testing, documentation, and on-going process control.

The test flow includes screening units with the defined flow (Class V and Q+ equivalent) and the appropriate periodic or lot conformance testing (Groups B, C, D, and E). Both the process and the products are subject to period or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests, respectively, as defined by Honeywell's Quality Management Plan.

Honeywell delivers products that are screened to two levels including Engineering Models and Flight Units. EMs are available with limited screening for prototype development and evaluation testing.

Group A	Final Lot Acceptance Electrical Tests
Group B	Mechanical – Dimensions (1), Bond Strength, Solvents, Die Shear, Solderability, Lead Integrity, Seal, Acceleration
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package related mechanical tests – Shock, Vibration, Accel, Salt (1), Seal, Lead Finish Adhesion, Lid Torque, Thermal Shock, Temp Cycle, Moisture Resistance
Group E	Radiation Tests

(1) Testing performed by package supplier.

Ordering Information

H	X	LVDS	D	G	V	F

Source
H = Honeywell

Process
X = SOI CMOS

Part Number

Part Type

Package Designation
G = 16 Pin Flat Pack

Screen Level
V = QML V
W = QML Q+
E = Eng. Model (2)

Total Dose Hardness
F = $3x10^5$ rad (Si)
N = No Level Guaranteed (2)

(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 for further information.
(2) Engineering Device Description: Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation guaranteed.

Standard Microcircuit Drawing

The HXLVDSD can be ordered under the SMD drawing 5962-07A02.

QCI Testing (1)

Classification	QCI Testing
QML Q+	No lot specific testing performed. (2)
QML V	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell QM Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

Find out more

To learn more about Honeywell's radiation hardened integrated circuit products and technologies, visit www.honeywell.com/microelectronics.

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